## DETAILED ACTION

1. This office action is in response to application 10/828,547 and response filed on 11/3/2008. Claims 2, 5 and 7-18 remain pending in the application.

### *Terminal Disclaimer*

2. The terminal disclaimer filed on 04/13/09 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the patent [6,453,446] has been reviewed and is accepted. The terminal disclaimer has been recorded.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2, 5 and 7-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kannan et al., "A Methodology and Algorithms for Post-Placement Delay Optimization," ACM, 31st ACM/IEEE Design Automation Conference, 1994, pp. 327-332.

5. As to claim 2, Kannan et al. an automated method for designing an integrated circuit layout with a computer (see entire document), comprising:

(a) selecting a plurality of cells that are intended to be used in the integrated circuit layout (Kannan et al. teach a placement-intelligent resynthesis methodology and optimization algorithms to meet post-layout timing constraints while at the same time reducing interconnect congestion [abstract]; cell libraries [Fig. 6 shows selection of cell

to be placed; Fig. 7 show a plurality of cells in cell libraries are selected for replacement];

(b) determining delay values for with the selected plurality of cells in order to satisfy delay constraints (section 2 describes placement-based timing analysis including delay calculations of selected cells in order to satisfy delay constraints in placement-based delay optimization described in section 3, by a placement-based synthesis system described in section 4; for example, placement-based delay optimization include insertion of buffers at p0 and p3 in Fig. 5(b) to satisfy delay constraints; the buffer configuration meets the timing constraints as shown in Fig. 5(b), see section 3.1 page 330]; and

(c) performing a placement of the selected plurality of cells after determining said delay values [Fig. 5(b) show placement of selected buffers at p0 and p3 in order to improve delay after calculation of delay values in section 2], the placement including assigning loads for the selected plurality of cells (Kannan et al. teach placement-based delay optimization including assigning precomputed loads and stored in section 2.1 (for example, precomputed and stored values of loads p1, p2, p4 and p5 shown in Fig. 5(b), in placement shown in Fig. 5(b) and determining a size or area of the selected plurality of cells in response to the said assigned loads and said delay values initial placement [sections 3 and 4 describe placement of buffers at p0 and p3 including assigning loads p1, p2, p4 and p5 that can be precomputed and stored at the nodes described in section 2.1; section 3.2 described gate resizing in order to improve delay to satisfy a number of design and technology constraints]. In addition, Kannan et al. teach the

buffer configuration that meets the timing constraints look like the one given in Fig. 5(b), see page 330. The buffer configuration includes characteristics (size or area and delay). In section 3.2, Kannan et al. teach gate resizing. In this teachnique, a cell is replaced with a cell in the library that is equivalent in functionality but having a better drive strength (determined size or area), intrinsic delay, load or other characteristic that makes it more appropriate [6] (page 330). The entire document applied.

6. As to claim 5, Kannan et al. teach determining the size or area of the cells that will approximately maintain said delay values determined prior to said placement (Fig. 5 and 6 show selected suitable buffers (having determined characteristics including delay and sizes) for placement will improve delay or approximately maintain the delay values). In addition, selected buffer configuration and placed as shown in Fig. 5(b) will meet timing constraints. Also, Kannan et al. teach as a preliminarily step to applying transformations, we strip off all the buffers and merge all redundant inverters introduced by the initial synthesis run. This will allow us to do a placement-based buffer insertion from scratch taking true wire parasitics into account (see section 3, page 329).

7. As to claim 7, Kannan et al. teach routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells (section 4 describes a placement based synthesis system and process shown in Fig. 10 and result of IC layout shown in Fig.11 below, where Fig. 11 shows an improved finalized size or area of generated IC layout using finalized size or area of the selected plurality of cells described in section 2-3).

8. As to claim 8, Kannan et al. teach, wherein said delay values are determined using gain (section 2 describes delay computation determined taking consideration of intrinsic gate delay, load delay, interconnect delay and slew sensitivity using gain; these parameters determine a gain of delay values by changing these parameter values).

9. As to claim 9, Kannan et al. teach, wherein said delay values are determined using logical effort (section 2 describes delay values are computed using logical effort, for example, same functionality of gate, by its delay values varied depending on parameter values used for delay calculation).

10. As to claim 10, Kannan et al. teach, wherein said delay values are determined by finding a preferred gain of the cells (section 2 described delays computed by finding a preferred gain of the cells using equation taking intrinsic gate delay, load delay, interconnect delay and slew sensitivity; these parameters are used to find a preferred gain of the cells; for exemple, a buffer configuration selected shown in Fig. 5(b) including size and delay, and of course a gain to satisfy timing constaints described on page 330).

11. As to claim 11, Kannan et al. teach, wherein the preferred gain of the cells is determined using a continuous buffering assumption (Fig. 4 and 5 and show suitable buffers are selected for placement for improving delay, equivalent buffers having continuous of sizes and delay values are determined and stored described in sections 2 and 3).

12. As to claim 12, Kannan et al. teach, wherein said delay values are determined during library analysis (see sections 2-4). Kannan et al. teach selected cells from cell library for placement to meet timing constraints (see section 3).

13. As to claim 13, Kannan et al. teach, wherein said delay values are determined using a typical load of the cells (see section 2). Kannan et al. teach delay calculation based on loads (see section 2).

14. As to claim 14, Kannan et al. teach, wherein the typical load is determined based on gain considerations (section 2). Fig. 5 show a buffer configuration selected based on loads improve delay and meet timing constraints (page 330). Section 2 described delay calculation using various parameters to determine delay values. By changing these parameter values, various delay values are obtained and a gain could be determined. That means a load could be determined based on gain considerations.

15. As to claim 15, Kannan et al. teach, wherein the size or area of the cells is variable and not fixed at the time the cells are selected (section 3 describes gate resizing, therefore selected buffers for placement including variable size or area providing a delay to meet timing constraints).

16. As to claim 16, Kannan et al. an automated method for designing an integrated circuit layout with a computer of a circuit specified by a netlist, comprising:
(a) providing a library of cells (Fig. 6 show component library for cell selection, for example, L is a component library for making selection of buffers or gates or cells; Fig. 8 show Gd library for making selection of buffers or gates or cells for placement or initial placement);

(b) determining initial delay values for a plurality of cells from said library of cells to be used in the integrated circuit layout of the circuit before determining an initial size or area of the cells, and using a timing driven covering method to map said plurality of cells to the circuit (section 2 describes delay computation in placement-based timing analysis; initial delay calculation is performed for a selected cell to be used for placement; for example, Fig. 5(b), a selected buffer having specific buffer configuration (size, delay) is given for placement for meet timing constraints, see page 330); and

(c) performing an initial placement of the cells, including assigning net lengths to nets on the cells, and determining the initial size or area of the cells in response to the initial placement (section 3 describes placement-based delay optimization including gate resizing; section 4 section describes an algorithm in placement-based resynthesis process). Kannan et al. teach: as a preliminarily step applying the transformations see strip off all the buffers and merge all redundant inverters introduced by initial synthesis run. This allow us to do a placement-based insertion from scratch taking true wire parasitics into account. We found that by including buffers in the initial placement, we can minimize changes in the net area of the components in the netlist. This improves chances that the incremental placer will find a solution close to the suggested placement (see section 3 starting page 329).

17. As to claim 17, Kannan et al. teach, inserting buffers based on an estimation of area savings in the circuit prior to determining said initial size or area of the cells (Fig. 5 show selected suitable buffers are inserted at p0 and p3; section 3 describes gate resizing). Section 3.1 describes insertion buffers based on an estimation of area saving

in the circuit. Fig. 5(b) show selected suitable buffers for placement and insertion at p0 and p3 and section 3.2 describes gate resizing, that means the insertion of buffers is prior determining initial size or area of the cells because the cells can be resized to fit an assigned die area after layout.

18. As to claim 18, Kannan et al. teach compressing or stretching delay values associated with cells prior to determining said initial delay values for the cells (section 4 describes stripping off all the buffers and removing all redundant cascades introduced by initial synthesis run that will allow do a placement-based buffer insertion taking true wire parasitics into account so that placement-based delay optimization can be done using fanout buffering and gate resizing transformations to reduce delay along critical paths in a network of IC design; section 3 describes that including buffers in initial placement will minimize changes in net area of components in the netlist while minimizing delay, that means stretching delay values).

19. Applicants are requested to consider entire document.

## *Remarks*

20. Applicant's arguments are moot in view of new ground of rejection. Applicants are requested to specifically point out each of claim limitations recited in the claims with support described in the disclosure.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
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